

FIG. 1

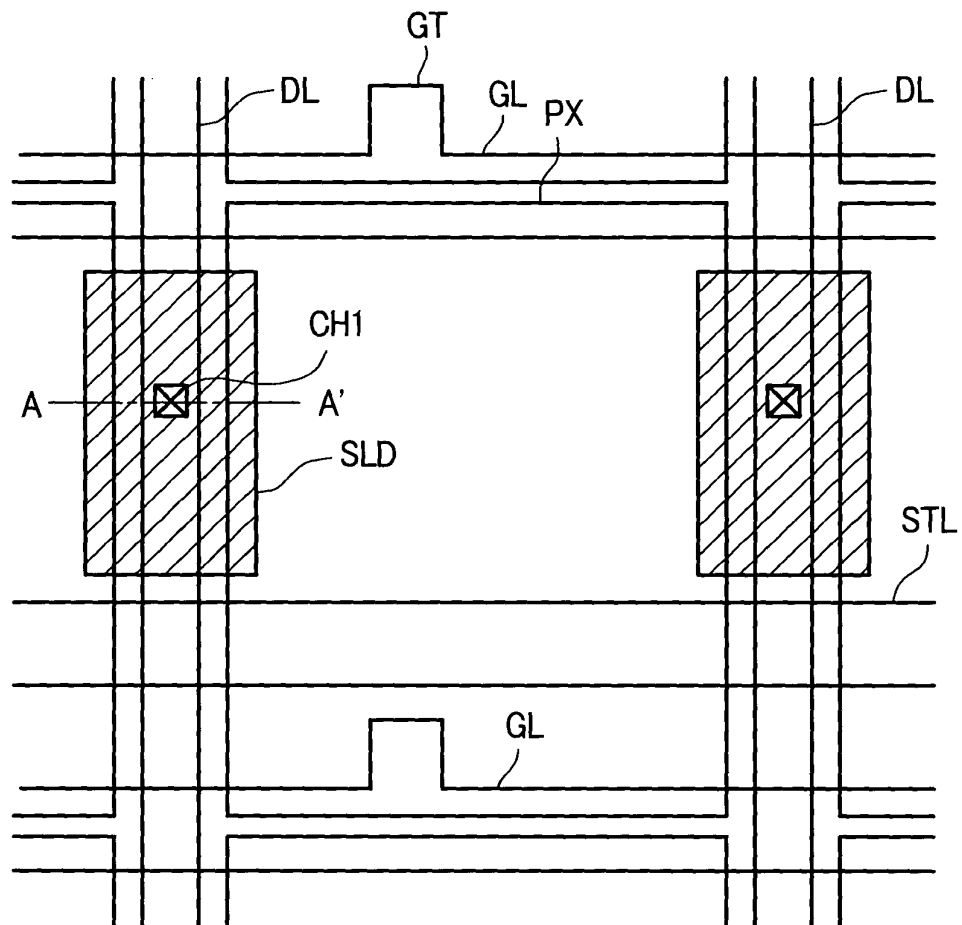


FIG. 2

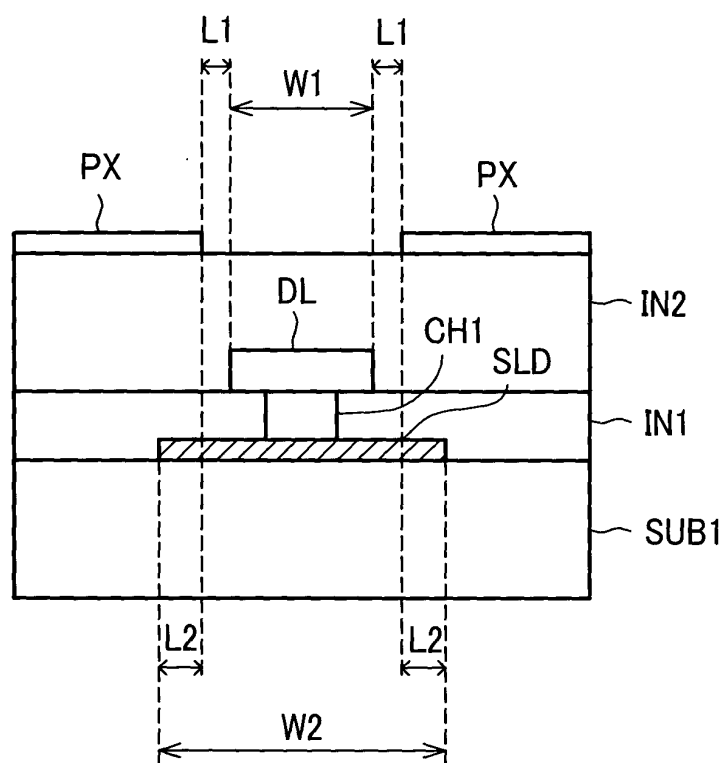


FIG. 3

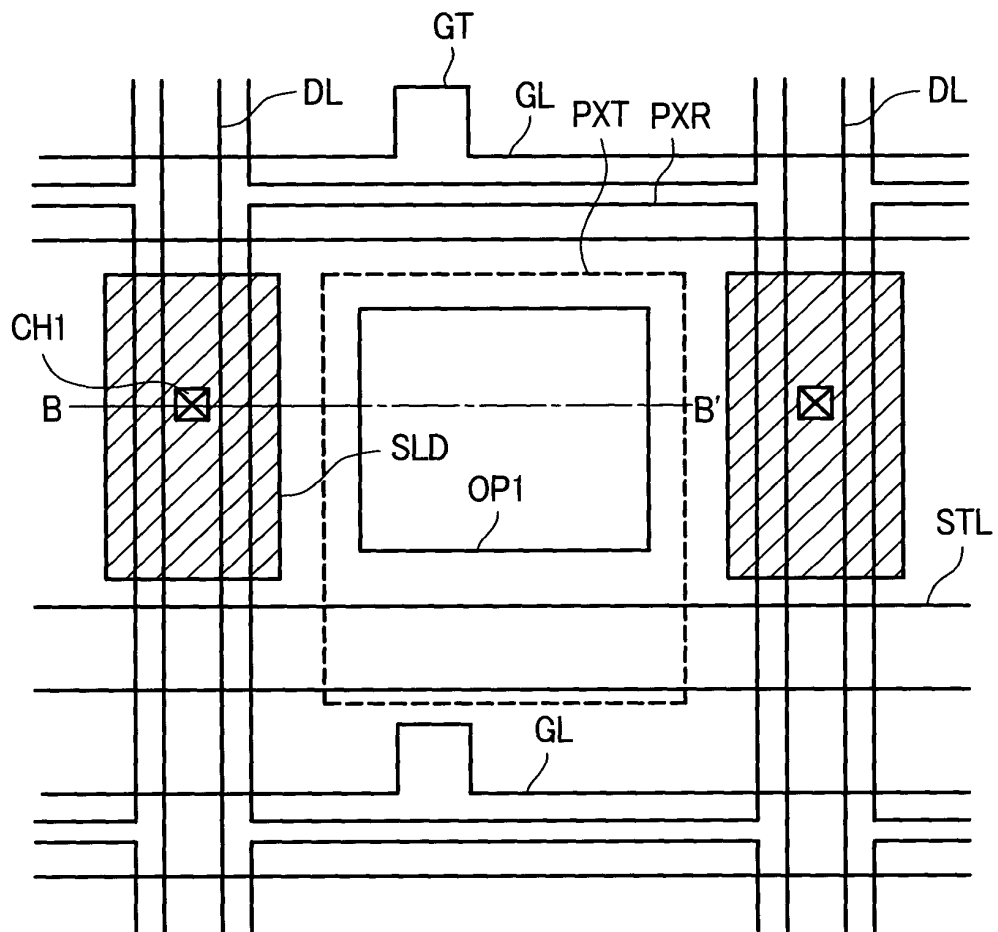


FIG. 4

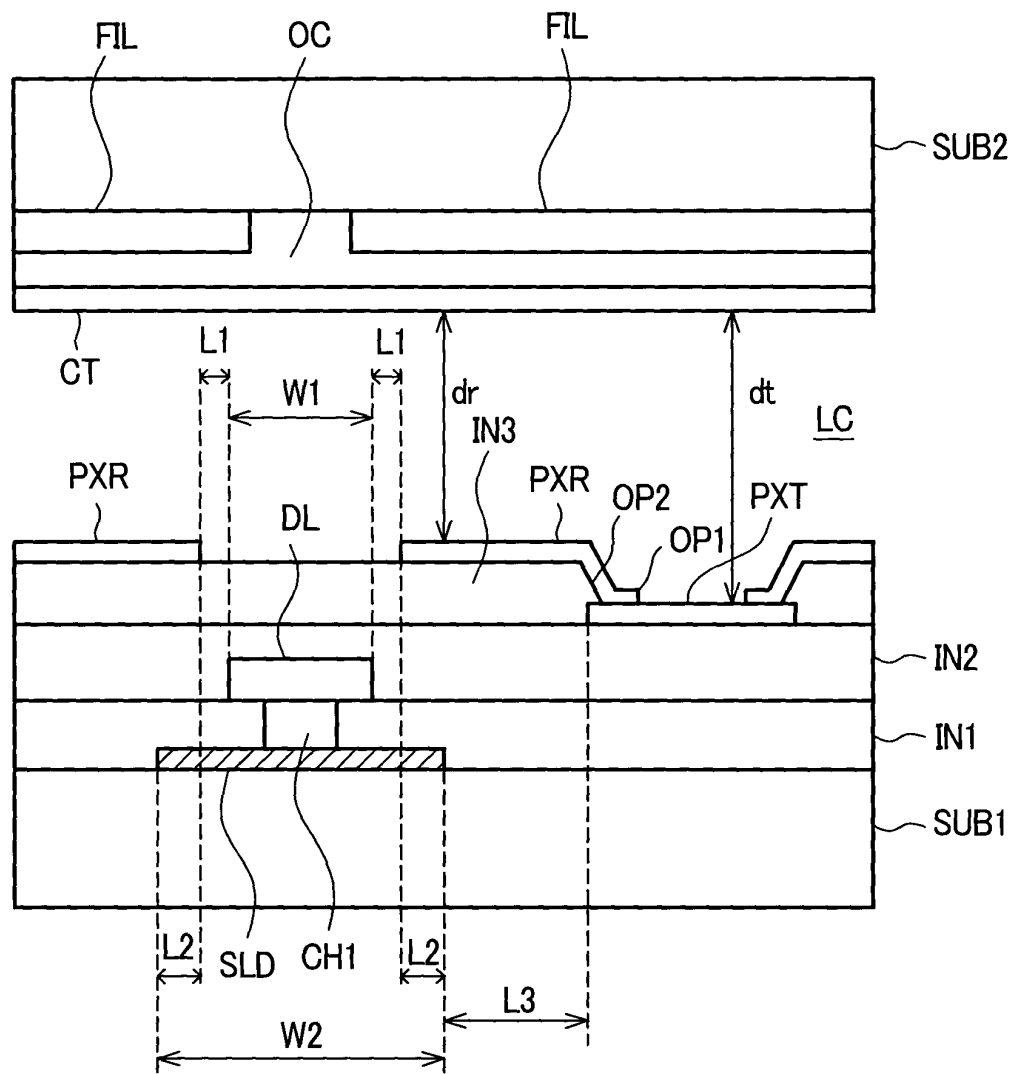


FIG. 5

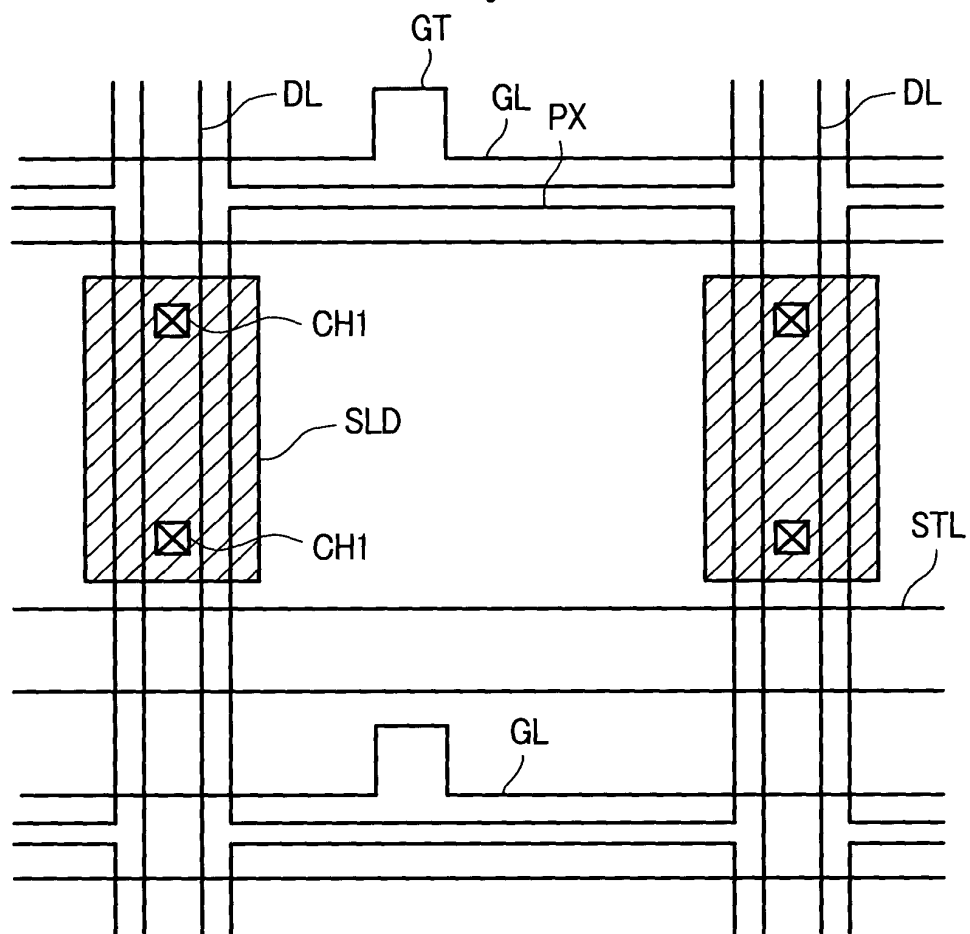


FIG. 6

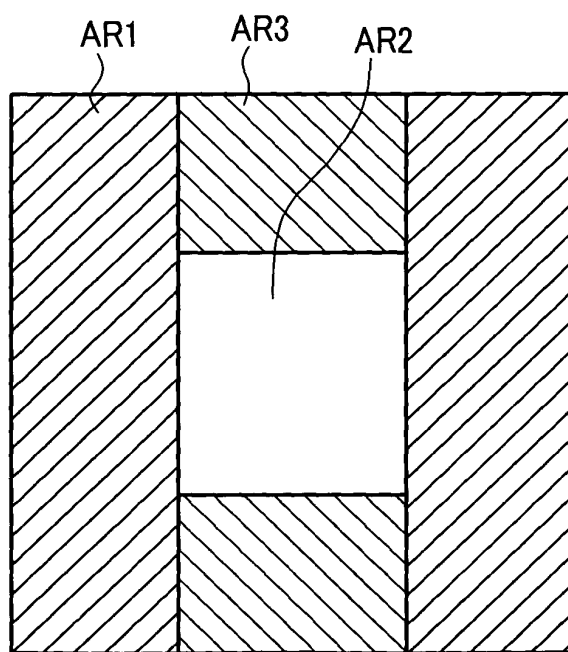


FIG. 7

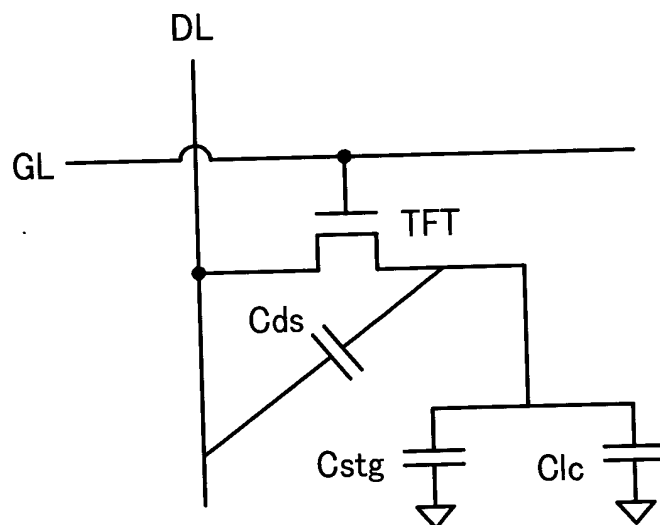


FIG. 8

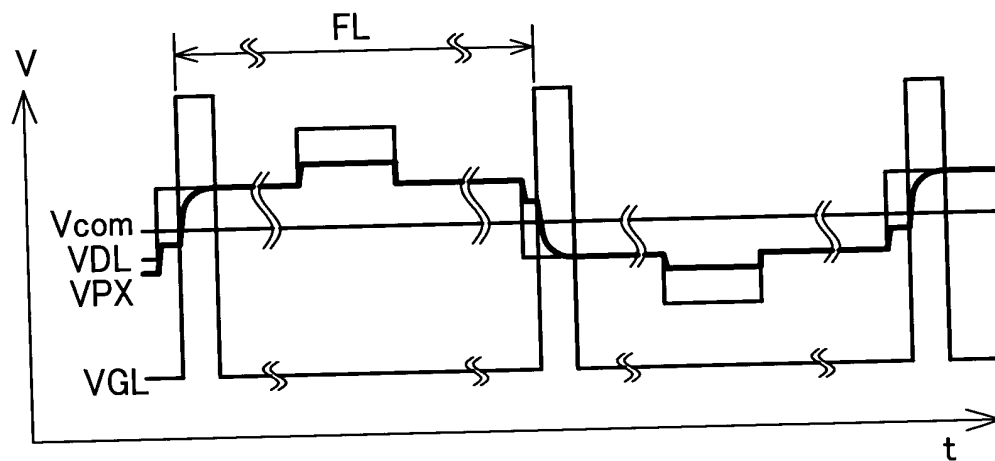


FIG. 9

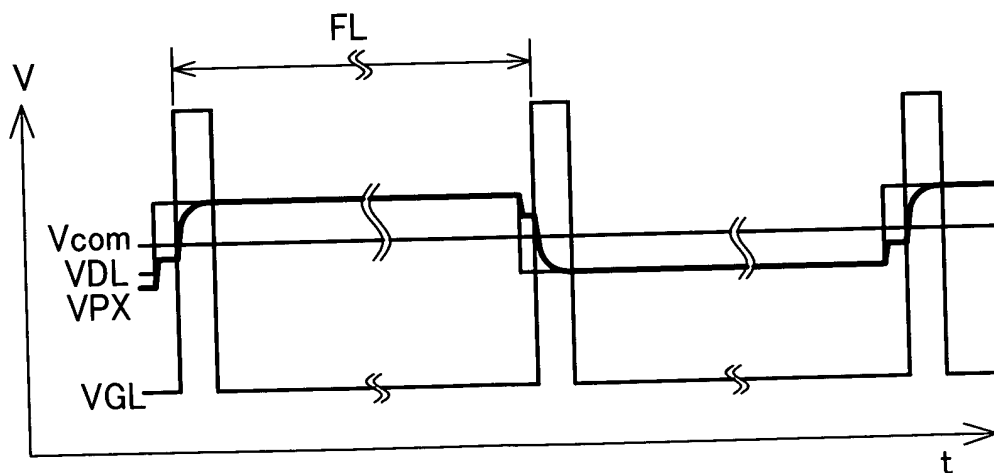


FIG. 10

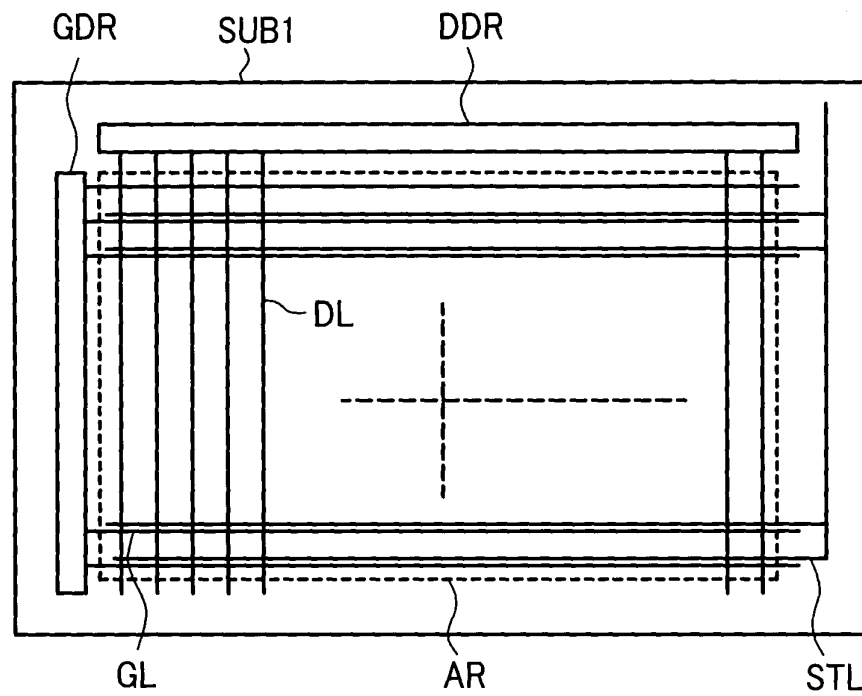


FIG. 11

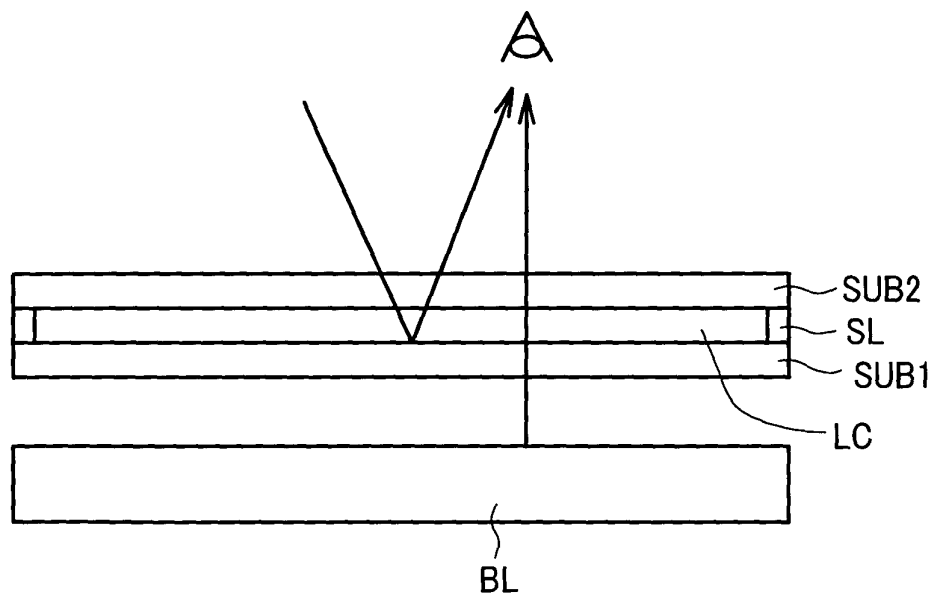
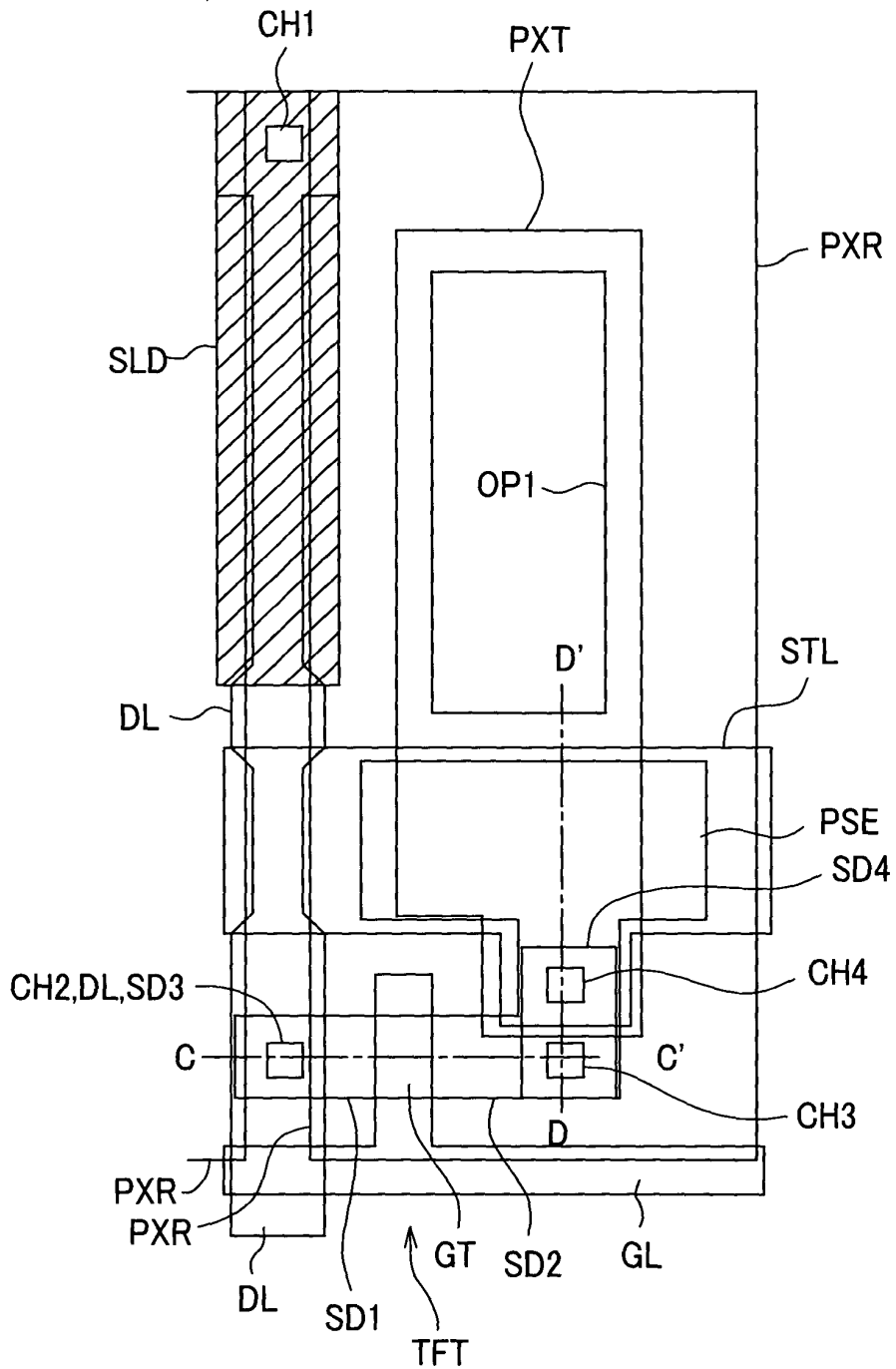


FIG. 12



A detailed cross-sectional view of a TFT-LED device. The structure is built on a substrate (SUB1) and includes a gate insulating layer (GI). A gate electrode (GT) is formed on the GI, with a passivation layer (PSC) and a protective layer (PXR) on top. The device features a TFT structure with a channel layer (CH2) and a source/drain region (SD1). A light-emitting layer (LED) is formed on the TFT, with a p-type layer (P) and an n-type layer (N). The LED is covered by a protective layer (PXR) and a passivation layer (PSC). The device is completed with a top layer (SD4) and a bottom layer (SD2). Labels include: DL,SD3; IN2; PXR; IN3; SD4; GI; SUB1; CH2; SD1; LDD; PSC; GT; LDD; IN1; SD2; CH3; and TFT.

A cross-sectional view of a semiconductor device. The structure consists of a substrate (SUB1) at the base. Above the substrate, there are several layers and structures. From bottom to top, the layers are labeled: IN1, STL, GI, PSE, CH3, SD2, and IN2. On the right side, there are two openings labeled OP1 and OP2. Above these openings, there are structures labeled PXR and PXT. In the center, there is a structure labeled CH4. At the top, there are two more layers labeled IN3 and SD4.

FIG. 15

Prior Art

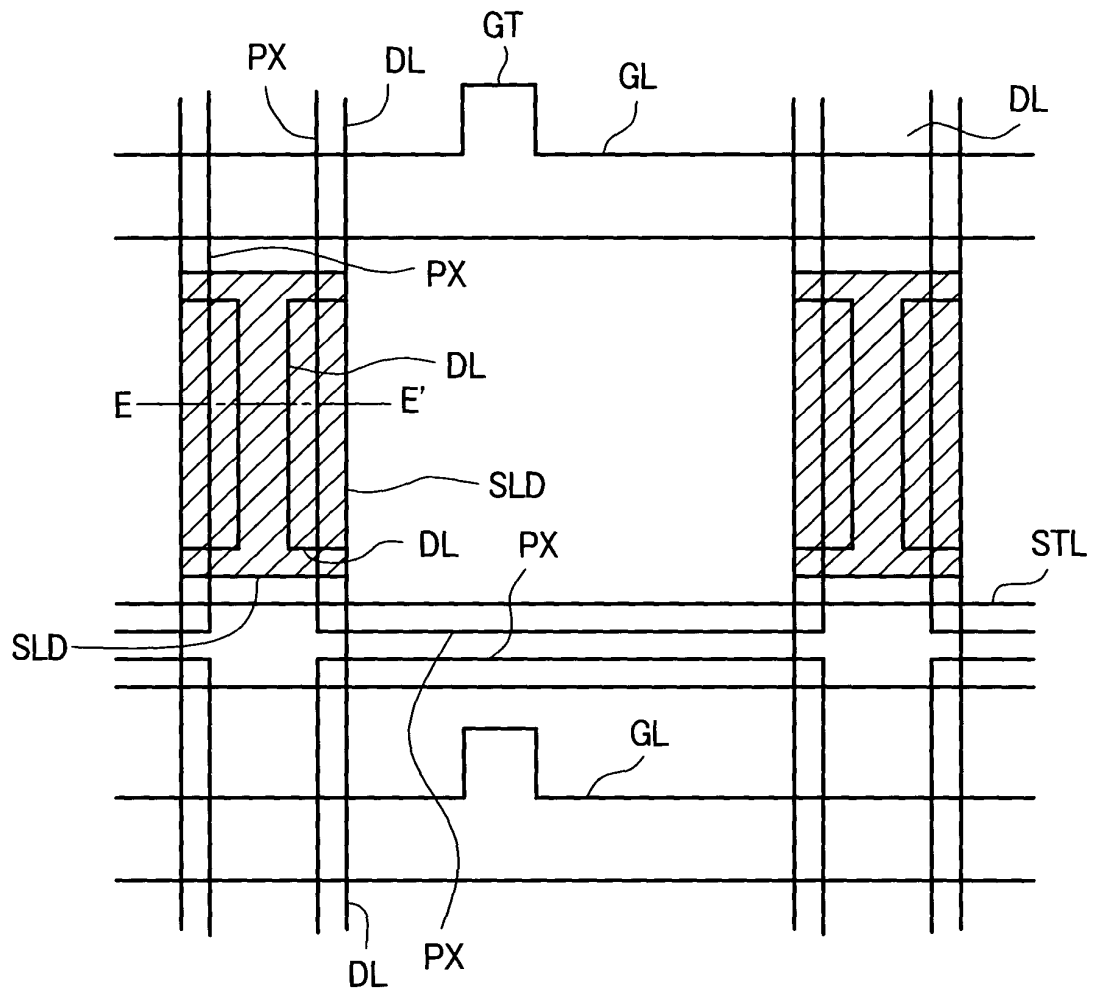
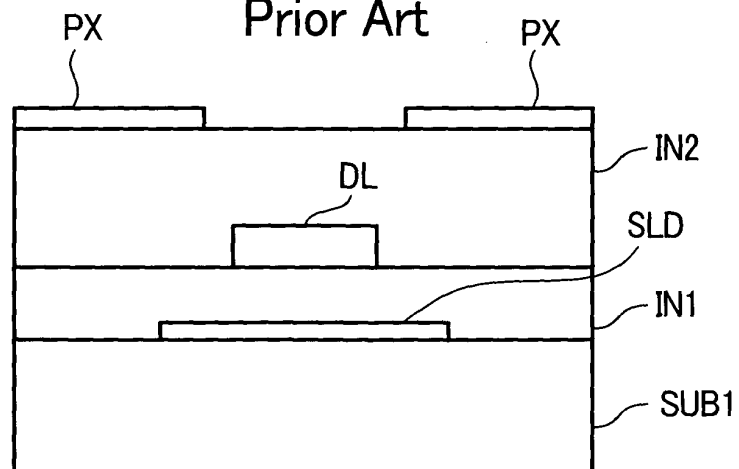


FIG. 16

Prior Art



Prior Art

